UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,136	09/09/2004	William C. Moyer	SC12888TH	3949

23125 7590 05/03/2005

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,136	MOYER ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-23 are in the application.

Claims 1-23 are rejected.

Information Disclosure Statement

2. The Information Disclosure Statements received 31 July 2003 has been considered. See attached PTO-1449(s).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8,10-12,15,~~18~~21-23 rejected under 35 U.S.C. 102 (e) as being anticipated by Phelps et al (US Pub 2004/0221111).

As in claim 1, Phelps describes data processing system (Fig 1), comprising: a first master (Fig 1: #20A); storage circuitry (Fig 1: system memory), coupled to the first master, for use by the first master; a first control storage circuit (Fig 1: #30A memory controller) which stores a first prefetch limit (number of pre-fetch read in Fig 5: #151 config storage); a prefetch buffer (Fig 5: #121 buffers, #110 cache memory); and prefetch circuitry (Fig 5: #150), coupled to the first control storage circuit, to the prefetch buffer, and to the storage circuitry, said prefetch circuitry selectively prefetches a predetermined number of lines from the storage circuitry into the prefetch buffer [Generally speaking, pre-fetch unit 150 controls whether data is pre-fetched into cache memory 110 and if so how much data is pre-fetched (i.e. how many cache lines; Phelps's page 4, paragraph 40], wherein the first prefetch limit controls how many prefetches occur between misses in the prefetch buffer [Configuration storage 151 may include a number of programmable locations that when selected may control both the number of pre-fetch read cycles that may be performed and the addresses that may be pre-fetched; Phelps's page 4, paragraph 41; determination logic 152 is configured to determine whether an incoming read request to a given address will cause cache subsystem 35 to return data associated with the read request to a requesting device or if the read request will generate one or more pre-fetch read cycles; Phelps's page 4, paragraph 42].

As in claim 2, it is rejected based on the same rationale as in the rejection of claim 1. The claim recites a counter to count the number of lines (read cycles) being read out from memory system. Phelps describes the configuration storage to perform read cycles to n+m addresses

[Phelps's page 4, paragraph 41]. Thus it's inherently that a counter is required to keep track the cycles being read.

As in claim 3, it is rejected based on the same rational as in claim 1. Phelps describes the data processing system of claim 1, further comprising: a second master (Fig 1: #20n), wherein the storage circuitry is coupled to the second master and is for use by the second master, and a second control storage circuit (Fig 1: #35b) which corresponds to the second master and stores a second prefetch limit [Turning now to FIG. 1, a block diagram of one embodiment of a multiprocessor computer system 10 is shown. Computer system 10 includes processors 20A and 20n coupled to memory subsystems 50, 50B and 50n via system bus 25. Each of memory subsystems 50A, 50B and 50n includes a memory controller 30A, 30B and 30n coupled to a system memory 40A, 40B and 40n via a memory bus 45A, 45B and 45n; Phelps's page 1, paragraph 16]

As in claim 4, it's rejected based on the same rationale as in claims 1 and 3.

As in claim 5, it's rejected based on the same rationale as in claims 2 and 3.

As in claim 6, the claim recites wherein the prefetch circuitry: selectively prefetches the predetermined number of lines for the first master based on the first prefetch counter in response to at least one of a hit or a miss in the prefetch buffer corresponding to an access request from the first master; and selectively prefetches the predetermined number of lines for the second master based on the second prefetch counter in response to at least one of a hit or a miss in the prefetch buffer corresponding to an access request from the second master. It is rejected based on the same rationale as in claims 1 and 3. Phelps further describes the determination logic which

determine whether incoming read request to a given address will cause cache subsystem to return data or if the read request will generate one or more prefetch read cycles (page 2 paragraph 42).

As in claim 7, it is rejected based on the same rationale as in claim 6.

As in claim 8, Phelps describes the data processing system of claim 1, wherein the first control storage circuit is programmable [Configuration storage 151 may include a number of programmable locations that when selected may control both the number of pre-fetch read cycles that may be performed and the addresses that may be pre-fetched; Phelps's page 2, paragraph 41, lines 1-3].

As in claims 10-11, they are rejected based on the same rationale as in claim 1.

Claim 12 rejected based on the same rationale as in claim 4.

As in claim 15, the rationale in the rejection of claim 1 is incorporated herein. Phelps further describe if the read request results in a miss, performing a demand fetch in response to the read request and setting the prefetch counter to a second value (read cycles of values n+m) [It is noted that a given received read request may generate a read request (corresponds to the claim's a demand fetch) and any number of pre-fetch read requests; Phelps's page 4, paragraph 42];

the claim further recites if the read request results in a hit, selectively performing a prefetch of a predetermined number of lines from the storage circuitry into the prefetch buffer based at least in

part on a prefetch counter reaching a first value (threshold), Phelps describes the prefech will be controlled by another threshold value [Phelp's page 4, paragraph 43];

As in claims 21-23, they are rejected based on the same rationale as in claim 15. Phelps clearly describes any number of lines may be prefetched (Phelps's paragraph 41)

As in claim 23, the claim recites the method of claim 15, further comprising: receiving a master identifier corresponding to the master', and selecting the prefetch counter from a plurality of prefetch counters based on the master identifier. Phelps describes a memory controller (Fig 1: #30A) capable of receiving read/write requests from multiple processors. Phelps further describes the system bus (Fig 2: #25) can be any type of network including broadcast network. Thus, Inherently the processors's identification must be broadcast on the bus and be received by the memory controller. [On the other hand, the address network may convey address information over a broadcast network in which address transactions are conveyed to all components. The address network of system bus 25 may be embodied physically using a point-to-point network, which may include switches. Both the address and data networks of system bus 25 may be implemented using a multi-stage switching hierarchy. System bus 25 may be implemented such that the address network is embodied in hardware that is separate from data network, or in hardware that is shared with the data network; Phelps's page 2, paragraph 19].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9,13,14,16-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Phelps et al (US Pub 2004/0221111) as applied to claims 1,10 and 15 respectively and in view of Bearden (US Pub 2004/0205299).

As in claim 9, the claim describes the data processing system of claim 1, further comprising a request monitor coupled to the first control storage circuitry, wherein the request monitor selectively updates the prefetch limit based on a number of buffer hits in the prefetch buffer accessed between two misses in the prefetch buffer. Note that in claim 1, the prefetch limit is used to determine a number of prefetch lines. Thus, the claim describes a request monitor that dynamically changes the number of prefetch lines. Phelps does not describe the claim's detail of the request monitor. However, Bearden describes a trigger method capable of monitoring the host read requests and dynamically changes the amount of prefech data [If the host is requesting

kB blocks of data in the small transfer length sequential workload, and the page size is 64 kB, the trigger module 410 will specify a pre-fetch up to the next 64 kB boundary; i.e., to the end of the page. Pre-fetching to the end of the page may amount to, for example, 32 kB. If the host continues to request sequential 2 kB blocks, corresponding read cache hits will continue to occur. Eventually, a read cache hit may occur at a tail portion (i.e., the end) of the page that was originally cached. The trigger module 410 may then trigger page sized pre-fetches; Bearden's page 7, lines 4-11]. It would have been obvious to one of ordinary skill in the art at the time of invention to include triggering scheme as suggested by Bearden in Phelps's system in order to give a flexibility to the amount of data to be prefetched in response to a host request [Any amount of data may be fetched in response to a read cache hit; Bearden's page 8, paragraph 88, lines 1-2].

Claims 13 and 14 are rejected based on the same rationale as in claim 9.

As in claims 16 and 17, they rejected based on the same rationale as in claim 9.

As in claim 18, the claim recites wherein the second value corresponds to a prefetch limit and wherein updating the counter comprises decrementing the prefetch counter. The claim appears to describe a situation of receiving a host request, which results in a prefetch buffer miss. Inherently, then the prefetch counter is preloaded with a prefetch limit value. Since this is a miss scenario, the storage circuitry will generate a demand fetch line for data of the host request and it will generate additional prefech lines. Thus the prefetch counter must be decrementing to adjust

(i.e. not include) for the demand fetch line. Phelps clearly describes the separation of demand fetch (read request) and additional fetches in paragraph 42.

As in claim 19, the claim recites wherein the first value corresponds to a prefetch limit and wherein updating the counter comprises incrementing the prefetch counter. The claim appears to describe a situation wherein the counter is used to record the outstanding prefetches to memory systems. Phelps clearly describe the outstanding prefetches must be kept tracked to dynamically adjust the prefetches to system memory [Phelps's page 4, paragraph 43].

As in claim 20, it is rejected based on the same rationale as in claim 19. The claim appears to describe when the outstanding prefech value of the counter reaches the total prefetch value, inherently; one should not prefetch any more lines.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 7/29/05

DD

Mano Padmanabhan

Supervisory Patent Examiner

TC2100

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER